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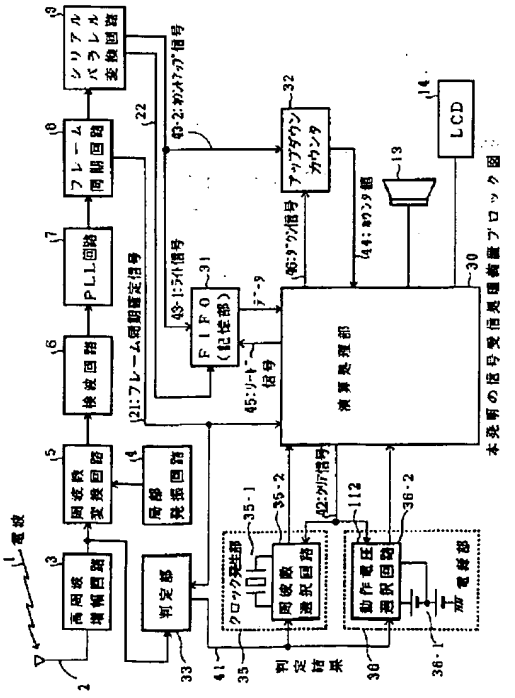
(54)【発明の名称】　信号受信処理装置

(57)【要約】

【目的】　演算処理部の発生する高周波ノイズの影響を十分に考慮して、効率的に入力信号処理を実行する。

【構成】　受信電波の強度が強い場合、クロック発生部３５は、クロック周波数を高くし、電源部３６は出力電圧を高める。信号強度が強いと、高周波ノイズの影響を受け難いので、高い処理速度で演算処理を実行させる。一方、受信電波の強度が弱い場合、クロック周波数を低下させて電源の出力電圧も低くし、高周波ノイズのレベルを十分低く抑える。このとき演算処理部３０の処理速度が低下するので、入力信号を一旦記憶部に蓄積し、処理速度低下を補償する。



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【特許請求の範囲】

【請求項1】　受信電波の強度を検出してそのレベルを判定する判定部と、

前記受信電波から得られたデータを処理する演算処理部と、

この演算処理部に対し2種以上の出力電圧のうちいずれかを選択して駆動用電力を供給する電源部と、

前記受信電波から得られた信号を、前記演算処理部が処理する前に一時蓄積する記憶部とを備え、

前記電源部は、

前記判定部により、前記受信電波の強度が強いと判定されたときは、高い出力電圧を選択し、前記受信電波の強度が弱いと判定されたときは、低い出力電圧を選択することを特徴とする信号受信処理装置。

【請求項2】　受信電波の強度を検出してそのレベルを判定する判定部と、

前記受信電波から得られたデータを処理する演算処理部と、

この演算処理部に対し2種以上の周波数の動作用クロックのうち何れかを選択して供給するクロック発生部と、

前記受信電波から得られた信号を、前記演算処理部が処理する前に一時蓄積する記憶部とを備え、

前記クロック発生部は、

前記判定部により、前記受信電波の強度が強いと判定されたときは、高いクロック周波数を選択し、前記受信電波の強度が弱いと判定されたときは、低いクロック周波数を選択することを特徴とする信号受信処理装置。

【請求項3】　受信電波の強度を検出してそのレベルを判定する判定部と、

前記受信電波から得られたデータを処理する演算処理部と、

この演算処理部に対し2種以上の出力電圧のうちいずれかを選択して駆動用電力を供給する電源部と、

前記演算処理部に対し2種以上の周波数の動作用クロックのうち何れかを選択して供給するクロック発生部と、

前記受信電波から得られた信号を、前記演算処理部が処理する前に一時蓄積する記憶部とを備え、

前記電源部は、

前記判定部により、前記受信電波の強度が強いと判定されたときは、高い出力電圧を選択し、前記受信電波の強度が弱いと判定されたときは、低い出力電圧を選択するとともに、

前記クロック発生部は、

前記受信電波の強度が強いと判定されたときは、高いクロック周波数を選択し、前記受信電波の強度が弱いと判定されたときは、低いクロック周波数を選択することを特徴とする信号受信処理装置。

【発明の詳細な説明】

【0001】

【産業上の利用分野】本発明は、無線を利用した呼出や

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警報等を行なうための信号受信処理装置に関する。

【0002】

【従来の技術】従来より、離れた場所にいるものに対する呼出や情報の伝達のための方法は、通信回線を利用した有線によるものの他、電波を利用した無線によるものがある。簡単な受信器を携帯し、電波によって呼出や簡単なメッセージの伝達等を行なうものも広く採用されている。また、ディジタル方式の信号処理によって情報伝達を行なうような装置も利用されている。

【0003】図2に、このような従来の信号受信処理装置のブロック図を示す。図の装置は、呼出や警報等の情報を載せた電波1をアンテナ2によって受信し、一定の処理を実行するものである。この装置には、高周波増幅回路3、局部発振回路4、周波数変換回路5、検波回路6、PLL回路7、フレーム同期回路8、シリアルパラレル変換回路9等が設けられ、受信電波から一定のデータを取り出す構成となっている。また、このデータを処理するために演算処理部10が設けられ、この演算処理部10は、電源部11及びクロック発生部12によって駆動されている。演算処理部10の処理結果は、ブザー13やLCD14に出力される構成となっている。

【0004】この装置により受信される電波は、中波に一定のフレーム形式のディジタルデータを載せて送られる。高周波増幅回路3は、アンテナ2で受信した微弱な電波を増幅し、周波数変換回路5に出力する。局部発振回路4は周波数変換回路5に対し、例えば455KHzの局部発振周波数の信号を出力し、周波数変換回路5は、これによって入力信号を中間周波に変換する。これは、良く知られたスーパーヘテロダイン方式の中波受信器の動作である。周波数変換回路5の出力は検波回路6に入力して復調される。

【0005】こうして、検波回路6からは一定のシリアルなディジタルパルス信号が得られるが、伝搬中に歪を生じた波形を整形するために、PLL回路7にこの信号が入力される。PLL回路は、いわゆるフェーズロックドループで入力信号を一定の周期を持つ一定のレベルのディジタル信号に整形する。フレーム同期回路8には、このPLL回路7の出力が入力する。このフレーム同期回路8によって入力信号のフレームの中から同期パルスを抽出し、フレーム中の信号処理のタイミングを得る。シリアルパラレル変換回路9は、このフレーム同期回路8の出力を受け入れて一定のビット幅でパラレルデータに変換し、演算処理部10に送り込む。

【0006】図3に受信電波からのデータ抽出処理説明図を示す。この図には、上記PLL回路7からフレーム同期回路8を経て、シリアルパラレル変換回路9によって入力信号をパラレルデータに変換する部分の動作を示した。即ち、PLL回路7の出力信号17は一定の長さのフレーム形式となっており、その先頭部分に同期信号17－1が含まれている。フレーム同期回路8は、この

同期信号１７－１から同期パルス２１－１を抽出し、入力信号１７の読取りタイミングを確定する。この同期確定信号２１は演算処理部１０に向け出力される。シリアルパラレル変換回路９は、こうして入力するシリアル信号を、例えば４ビットあるいは８ビットずつ切り出してパラレルデータ２２に変換し、演算処理部１０に送り込む。

【０００７】演算処理部１０は、こうして得られたデータを解読して分析し、例えばその内容をＬＣＤ（液晶表示装置）１４に表示したり、必要に応じてブザー１３を鳴らす。なお、電源部１１は電池１１－１を備えており、スイッチ１１－２をオンすることによって演算処理部１０に駆動用電力を供給する回路である。また、クロック発生部１２は、クロック発振器１２－１を備えており、演算処理部１０の演算動作のためのクロックを供給する回路である。

【０００８】

【発明が解決しようとする課題】ところで、上記のような従来の信号受信処理装置では、演算処理部１０から発生する高周波ノイズ１６がアンテナ２によって受信され、本来受信しようとする電波１を妨害するといった問題があった。そこで、従来、クロック発生部１２の発生するクロック周波数を、例えば数十ＫＨｚ程度まで低くすることによって高調波成分を減少させ、妨害の抑制を図っている。また、電源部１１の出力電圧は３Ｖ以下に設定し、クロックの信号レベルも低下させて高周波ノイズのエネルギーを減少させるようにしている。

【０００９】しかしながら、このような解決を図る場合、例えば高速転送速度で情報量を多くしようとすると、演算処理部１０における処理が間に合わなくなる。即ち、クロック発生部１２におけるクロックの周波数を高くして信号処理速度をアップしなければ入力した情報の処理が間に合わない。従って、受信電波の強度が十分強い場合以外は高周波ノイズの影響を無視できず、情報量を増やすことができないといった問題があった。

【００１０】本発明は以上の点に着目してなされたもので、演算処理部の発生する高周波ノイズの影響を十分に考慮して、効率的に入力信号処理を実行する信号受信処理装置を提供することを目的とするものである。

【００１１】

【課題を解決するための手段】本発明の第１発明は、受信電波の強度を検出してそのレベルを判定する判定部と、前記受信電波から得られたデータを処理する演算処理部と、この演算処理部に対し２種以上の出力電圧のうちいずれかを選択して駆動用電力を供給する電源部と、前記受信電波から得られた信号を、前記演算処理部が処理する前に一時蓄積する記憶部とを備え、前記電源部は、前記判定部により、前記受信電波の強度が強いと判定されたときは、高い出力電圧を選択し、前記受信電波の強度が弱いと判定されたときは、低い出力電圧を選択することを特徴とする信号受信処理装置に関する。

【００１２】第２発明は、受信電波の強度を検出してそのレベルを判定する判定部と、前記受信電波から得られたデータを処理する演算処理部と、この演算処理部に対し２種以上の周波数の動作用クロックのうち何れかを選択して供給するクロック発生部と、前記受信電波から得られた信号を、前記演算処理部が処理する前に一時蓄積する記憶部とを備え、前記クロック発生部は、前記判定部により、前記受信電波の強度が強いと判定されたときは、高いクロック周波数を選択し、前記受信電波の強度が弱いと判定されたときは、低いクロック周波数を選択することを特徴とする信号受信処理装置に関する。

【００１３】第３発明は、受信電波の強度を検出してそのレベルを判定する判定部と、前記受信電波から得られたデータを処理する演算処理部と、この演算処理部に対し２種以上の出力電圧のうちいずれかを選択して駆動用電力を供給する電源部と、前記演算処理部に対し２種以上の周波数の動作用クロックのうち何れかを選択して供給するクロック発生部と、前記受信電波から得られた信号を、前記演算処理部が処理する前に一時蓄積する記憶部とを備え、前記電源部は、前記判定部により、前記受信電波の強度が強いと判定されたときは、高い出力電圧を選択し、前記受信電波の強度が弱いと判定されたときは、低い出力電圧を選択するとともに、前記クロック発生部は、前記受信電波の強度が強いと判定されたときは、高いクロック周波数を選択し、前記受信電波の強度が弱いと判定されたときは、低いクロック周波数を選択することを特徴とする信号受信処理装置に関する。

【００１４】

【作用】この装置では、受信電波の強度が強い場合、クロック発生部はクロック周波数を高くし、電源部は出力電圧を高める。信号強度が強い場合、高周波ノイズの影響を受け難いので、これによって高い処理速度で演算処理を実行させる。逆に受信電波の強度が弱い場合、クロック周波数を低下させて電源の出力電圧も低くし、高周波ノイズのレベルを抑える。入力信号が高速転送モードの場合、これを一旦記憶部に蓄積し、演算処理部の処理速度低下を補償する。

【００１５】

【実施例】以下、本発明を図の実施例を用いて詳細に説明する。図１は、本発明の信号受信処理装置実施例を示すブロック図である。図の装置は、図２を用いて説明した従来の装置と同様に、アンテナ２、高周波増幅回路３、局部発振回路４、周波数変換回路５、検波回路６、ＰＬＬ回路７、フレーム同期回路８、シリアルパラレル変換回路９を備えている。また、これらの回路により得られたデータを処理するために演算処理部３０が設けられ、その処理結果はブザー１３やＬＣＤ１４に出力される構成となっている。ここまでの構成は、従来の装置と変わるところはない。ここで、本発明の装置には、シリ

アルパラレル変換回路9の出力するデータ22を一時格納するためにFIFO（先入れ先出しメモリ）31が設けられている。本発明では、このFIFO31を記憶部と呼んでいる。また、このFIFO31に格納されたデータを管理するためにアップダウンカウンタ32が設けられている。

【0016】一方、高周波増幅回路3の出力は、周波数変換回路5に向けて出力される他、受信電波の強度を検出してそのレベルを判定するための、判定部33に入力するよう構成されている。また、この判定部33の出力する判定結果41は、クロック発生部35及び電源部36に入力するよう構成されている。クロック発生部35には、クロック発振器35－1と周波数選択回路35－2が設けられている。周波数選択回路35－2は、演算処理部30に供給するクロックの周波数を、例えばこの実施例では2段階に切り換え、高い周波数と低い周波数のクロックのいずれか一方を選択して出力できる構成となっている。この周波数の選択用回路は、例えば周波数変換回路35－2に設けられた分周回路の出力を選択するスイッチ等により構成される。これにより、例えばこのクロック発生部35は、従来と同様の数十KHzの低い周波数のクロックと、その2倍あるいは数倍のクロックのいずれかを選択して出力できる構成となっている。

【0017】一方、電源部36には電池36－1と動作電圧選択回路36－2が設けられている。この動作電圧選択回路36－2は、電池36－1の出力をスイッチにより切り換え、例えば3Vと4．5Vの2種類の出力電圧のうち、いずれか一方を選択して出力できる構成とされている。なお、フレーム同期回路8からは、従来装置と同様フレーム同期確定信号21が出力されるが、この信号は判定部33にも入力し、判定部33は、このフレーム同期確定信号21の入力するタイミングで判定結果41を出力する構成とされている。判定部33は、具体的には高周波増幅回路3の出力する信号を一定の基準値と比較する比較回路と、その比較結果をフレーム同期確定信号21の制御によってクロック発生部35や電源部36に出力するゲート回路等から構成される。

【0018】FIFO31は、シリアルパラレル変換回路9から出力されるデータを、そのライト信号43－1の入力するタイミングで受け入れ、順番に蓄積するメモリから構成される。こうして蓄積されたデータは、演算処理部30から出力されるリード信号45によって演算処理部30へ向けて読み出される。このFIFO31の記憶容量は、入力信号の情報量が演算処理部30の単位時間当りの情報処理量を超えた場合に、その過剰な分を蓄積できる適当な量に設定する。アップダウンカウンタ32は、シリアルパラレル変換回路9から出力されるカウントアップ信号43－2を受け入れ、FIFO31にデータが1個格納される度にそのカウンタ値を1ずつアップし、演算処理部30がFIFO31からデータを1個読み出すごとにダウン信号46の入力によって、そのカウンタ値を1ずつダウンさせるよう構成されたカウンタである。アップダウンカウンタ32の出力するカウンタ値44は演算処理部30に向け出力され、演算処理部30は、このカウンタ値44によってFIFO31の中に格納された残りのデータの量を認識できる構成となっている。

【0019】なお、クロック発生部35と電源部36には、いずれも周波数選択回路35－2や動作電圧選択回路36－2の動作を初期値に戻すため、クリア信号42が入力するよう構成されている。演算処理部30は、このクリア信号42を所定のタイミングでクロック発生部35や電源部36に向け出力し、初期状態を設定するよう構成されている。

【0020】以下、本発明の装置の動作を説明する。まず、電源部36の図示しないスイッチを接続すると、回路に予め設定された初期状態の出力電圧で電力が供給される。この電圧は、例えば低い方のレベルに設定されているものとする。また、クロック発生部35は、初期状態として低い方のクロック周波数でクロックを発生し、演算処理部30に供給する。ここで、アンテナ2によって電波1を受信すると、高周波増幅回路3がその電波を増幅する。その出力は周波数変換回路5及び判定部33に入力する。周波数変換回路5は局部発振回路4の出力によって中間周波を生成し、検波回路6は、その信号を復調する。PLL回路7は入力信号の波形を整形し、フレーム同期回路8において同期処理が実行される。これらは、既に図2を用いて説明した従来の装置と同様の動作である。

【0021】ここで、フレーム同期回路8からフレーム同期確定信号21が出力されると、先に説明したように判定部33は、そのタイミングで高周波増幅回路3の出力する信号のレベルを判断した判定結果41をクロック発生部35及び電源部36に出力する。クロック発生部35の周波数選択回路35－2及び電源部36の動作電圧選択回路36－2は、この判定結果41に従って、それぞれクロックの周波数及び出力電圧を選択する。従って、例えば受信電波のレベルが低い場合には、演算処理部30を駆動する電圧は低く、またその信号処理のためのクロック周波数は低いままに維持される。一方、受信電波の強度が強い場合、電源部36の出力電圧がアップし、クロック発生部35の発生するクロック周波数が高く設定されて、演算処理部30は高速モードで動作を行なう。

【0022】図4に、本発明の装置の高速モードにおける動作タイムチャートを示す。図の（a）に示すように、受信データが時刻t1に受信され、（b）に示すように、フレーム同期確定信号が時刻t2にフレーム同期回路8から出力されたものとする。この場合、クロック発生部35及び電源部36が、図4の（c）、（d）に

示すようにクロック周波数及び動作電圧を選択する。この例では、クロック周波数が高速に選択され、動作電圧が高電圧に選択される。

【0023】この状態で、シリアルパラレル変換回路9は、ＦＩＦＯ31に向けてパラレル変換したデータの書き込みを行なう（同図（ｅ））。演算処理部30には、フレーム同期回路8からフレーム同期確定信号21が入力しており（同図（ｆ））、演算処理部30は、そのタイミングでＦＩＦＯ31からデータの読出しを開始する。受信データのフレームは、図4（ａ）に示すように時刻ｔ1～時刻ｔ4の間受信されるが、演算処理部30は時刻ｔ2から高速モードにおいてデータを処理し、時刻ｔ5に、その処理結果に基づいてブザー13を駆動したり、ＬＣＤ14に処理結果の表示を行なう（同図（ｈ））。演算処理部30は処理が終了すると、時刻ｔ6にクリア信号42を出力し、クロック発生部35及び電源部36のクロック周波数や動作電圧の切換えを指示する（同図（ｇ））。

【0024】このように、初期値を低い出力電圧で低いクロック周波数に設定するのは、受信電波の強度を判定する場合に、その演算処理部30の発生する高周波ノイズを十分に低くし、誤った判定を行なわないようにするためである。例えば、上記演算処理部30には、通常8ビットあるいは4ビットのマイクロコンピュータが使用される。その動作クロックは、1ＭＨｚ～5ＭＨｚ程度の範囲であるが、この種の信号受信処理装置においては、高周波ノイズを十分低く抑えるために、クロック周波数を数十ＫＨｚに選定していた。なお、この場合、電源電圧は1．5Ｖ～3Ｖ程度に設定されていた。

【0025】このような状態では、データの転送速度が最大でも512ｂｐｓ程度に制限される。しかしながら、例えばデータ転送速度が4800ｂｐｓ程度の場合、クロック周波数を数ＭＨｚ程度に選定しなければ処理が間に合わない。また、この種のデータは、スクランブル処理、即ち、データビットのハイあるいはローの状態が続くとＰＬＬが動作しないため、ハイとローが均等に散らばるようにデータをコード化するための処理が行なわれる。従って、このようなデータの解読後、エラー訂正処理等を実行し、その後に実際のデータ処理が実行されるため処理量が多く、動作クロックが遅い場合、応答自体も著しく遅くなってしまう。従って、上記のような高速モードでの動作を可能にすることによって、このような問題を解決できる。

【0026】一方、受信電波の強度が弱い場合には、本発明の装置は次のように動作する。図5に、本発明の装置の低速モードにおける動作タイムチャートを示す。図5（ａ）に示すように、時刻ｔ1～時刻ｔ3の間、データの受信が行なわれ、時刻ｔ2にフレーム同期確定信号が出力されるものとする（同図（ｂ））。この場合に、受信電波の強度が弱ければ、判定部33の判定結果41に従って、クロック発生部35は低い周波数のクロックを選択し、電源部36は低い電圧を選択して演算処理部30に供給する（同図（ｃ）、（ｄ））。これによって、演算処理部30の発生する高周波ノイズは、十分低いレベルに設定され、受信電波に対する妨害を抑制される。

【0027】一方、演算処理部30はクロック周波数の低下によってその処理速度が低下する。従って、シリアルパラレル変換回路9から出力されるデータをそのまま受け入れては処理が間に合わないケースが発生する。そこで、ＦＩＦＯ31にシリアルパラレル変換回路9から入力するデータが一旦蓄積され、演算処理部30は設定された処理速度に従って、そのデータをＦＩＦＯ31から呼び出して処理する。その関係は図5（ｅ）と（ｆ）に示すようになる。即ち、ＦＩＦＯ31には受信されたデータが時刻ｔ3までに格納されるが、演算処理部30は、その後時刻ｔ4までの間にデータを読出し演算処理を実行する。アップダウンカウンタ32は、この間ＦＩＦＯ31に格納されたデータの量をカウントし（同図（ｇ））、演算処理部30は読み出すべきデータの量を管理する。その結果、演算処理部30の処理結果は、時刻ｔ5にブザー13やＬＣＤ14に出力される（同図（ｉ））。

【0028】図4及び図5を比較してわかるように、クロック周波数を低く切り換えることによって演算処理速度は低下し、装置の応答速度が遅くなるが、受信データがＦＩＦＯ31に一時的に記憶されるために、演算処理部30は確実に動作し、必要な処理結果を出力する。従って、電界が弱い場所において、ノイズによって信号の受信誤りを生じたり、あるいは信号の転送速度が早いために処理が間に合わなくなって誤動作するといった障害も防止できる。

【0029】本発明は以上の実施例に限定されない。上記実施例においては、受信電波のレベルが高い場合と低い場合とで、クロック発生部35の出力するクロックの周波数と電源部36の出力電圧を同時に高くしたり、低くしたりするように切換えを行なった。しかしながら、例えば電源部36の出力する電源電圧を一定にし、クロック発生部35の出力するクロックの周波数のみを換えるようにしても差し支えない。その切換え段数は2段階でなく、3段階以上自由に切り換えられるようにしてもよい。従って、演算処理部30の出力する高周波ノイズの影響が大きくない範囲で、クロック発生部35の出力するクロック周波数や電源部36の出力電圧を、それぞれ個々に独立に何段階かに切り換えて、最適な状態で演算処理部30を駆動するように構成してもよい。また、受信回路の構成は、電波により送られる信号の性質によって自由に変更して差し支えなく、記憶部やクロック発生部、電源部等の制御方法は、その回路構成によって自由に変更することができる。また、演算処理部の処理結

果はブザーやＬＣＤ等に表示する場合の他、その結果に基づいて直接何らかの装置の動作を制御するようなものについても本発明が適用できる。

【００３０】

【発明の効果】以上説明した本発明の信号受信処理装置は、受信電波の強度を検出して判定部によりそのレベルを判定し、受信電波の強度が強い場合には、電源部の出力電圧が高く選択され、またクロック発生部のクロック周波数が高く選択され、受信電波の強度が弱い場合には、電源部の出力電圧が低く選定され、クロック発生部の出力するクロック周波数が低く選択されるので、常に演算処理部の発生する高周波ノイズを受信動作に影響しないレベルに抑え、確実な信号処理を行なうことができる。従って、受信電波の強度が高い場合、高速で信号処理を行なうことができ、大量の情報を速やかに処理することができる。また、受信電波の強度が弱い場合、自動的に高周波ノイズを低く抑え、処理速度の低下は記憶部にデータを一時蓄積することによって補うため、動作が確実となる。

【００３１】更に、通常の状態では、クロック周波数と動作電圧を低くしておくため消費電力が軽減され、電池等を用いて駆動する場合には、その動作可能時間を長くすることができる。また、クロック周波数のみを調整した場合には、演算処理部の動作上あるいは高周波ノイズ軽減効果から見て、その調整範囲に限界があるが、クロック周波数と電源電圧を同時に変化させることによって、広い範囲で動作モードを選択できる効果もある。また、動作電圧のみを変化させる簡単な制御によっても、一定の範囲で高周波ノイズを調整し、最適な状態での受信動作を確保できる。

【図面の簡単な説明】

【図１】本発明の信号受信処理装置実施例を示すブロック図である。

【図２】従来の信号受信処理装置ブロック図である。

【図３】受信電波からのデータ抽出処理説明図である。

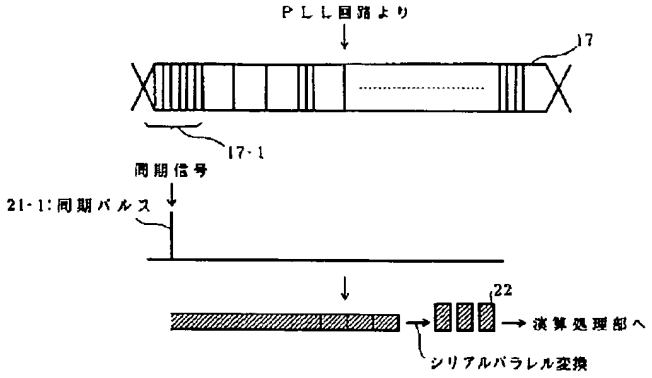
【図４】本発明の装置の高速モードにおける動作タイムチャートである。

【図５】本発明の装置の低速モードにおける動作タイムチャートである。

【符号の説明】

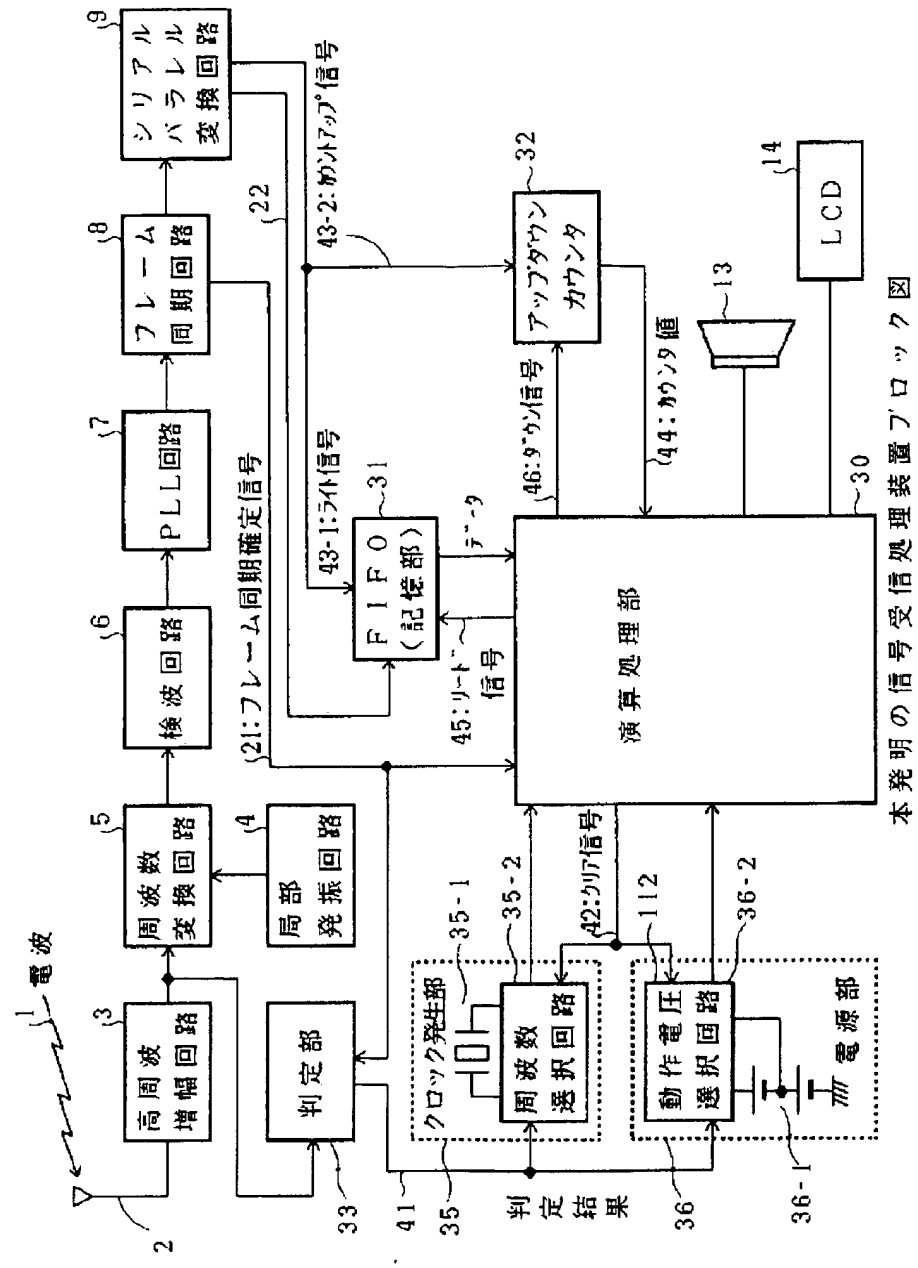
３０　演算処理部
３１　ＦＩＦＯ（記憶部）
３３　判定部
３５　クロック発生部
３６　電源部

【図３】

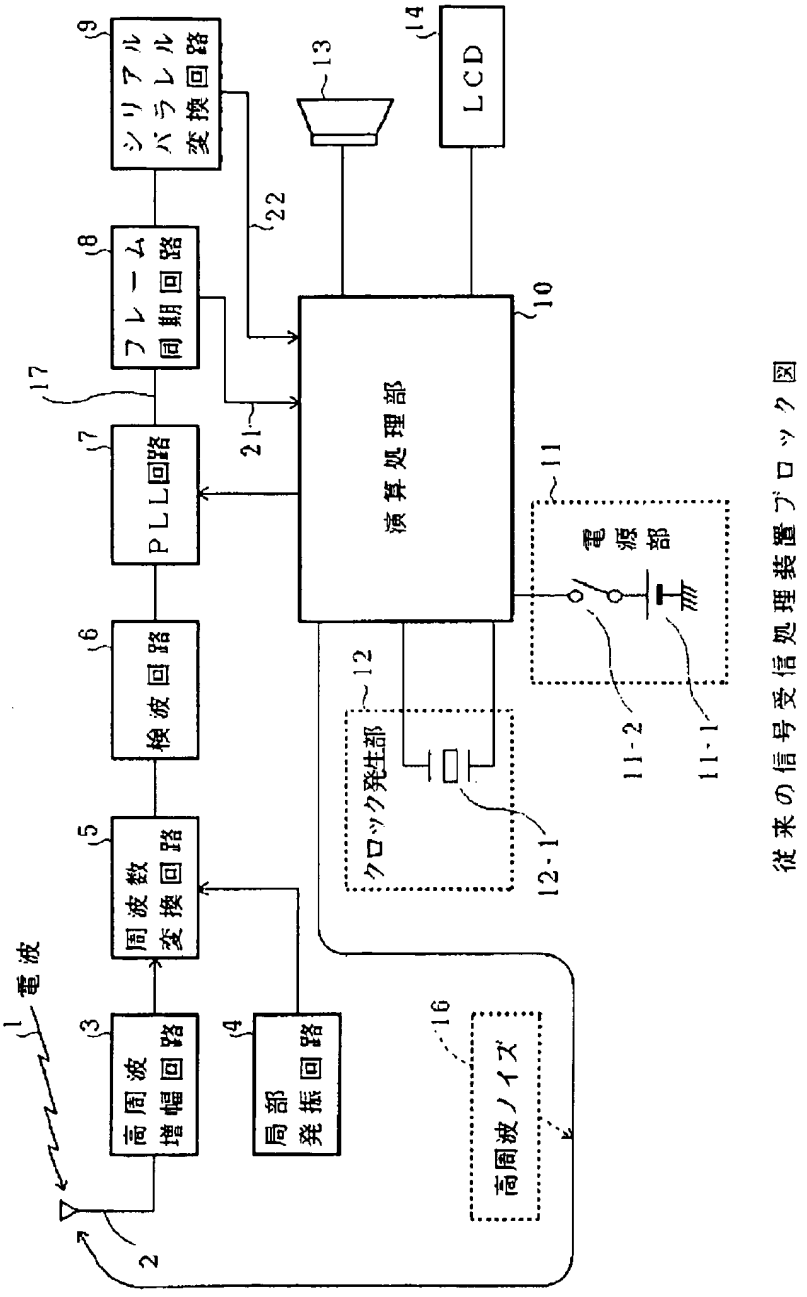


受信電波からのデータ抽出処理説明図

【図1】

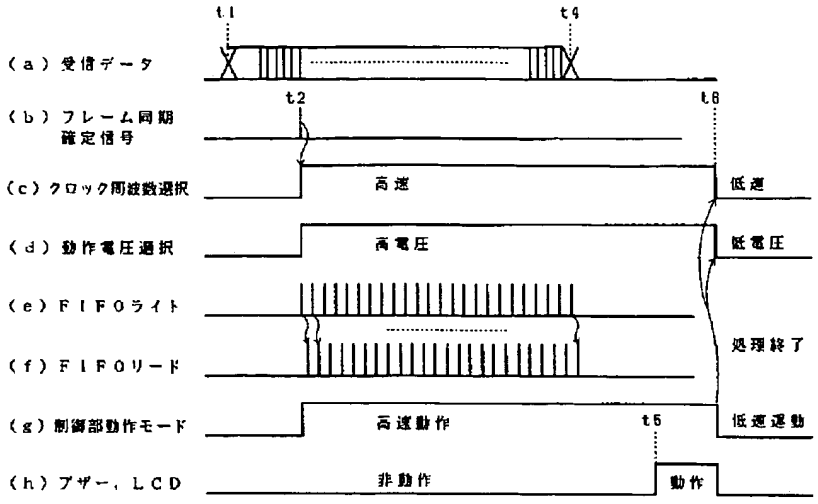

電波
1
2
高周波増幅回路
3
周波数変換回路
5
局部発振回路
4
検波回路
6
PLL回路
7
フレーム同期回路
8
シリアルパラレル変換回路
9
判定部
33
22
21:フレーム同期確定信号
43-1:ライト信号
43-2:カウントアップ信号
FIFO（記憶部）
31
データ
45:リード信号
演算処理部
30
46:ダウン信号
44:カウンタ値
アップダウンカウンタ
32
13
LCD
14
クロック発生部
35-1
35-2
周波数選択回路
42:クリア信号
112
動作電圧選択回路
36-2
電源部
41
35
判定結果
36
36-1
本発明の信号受信処理装置ブロック図

【図2】



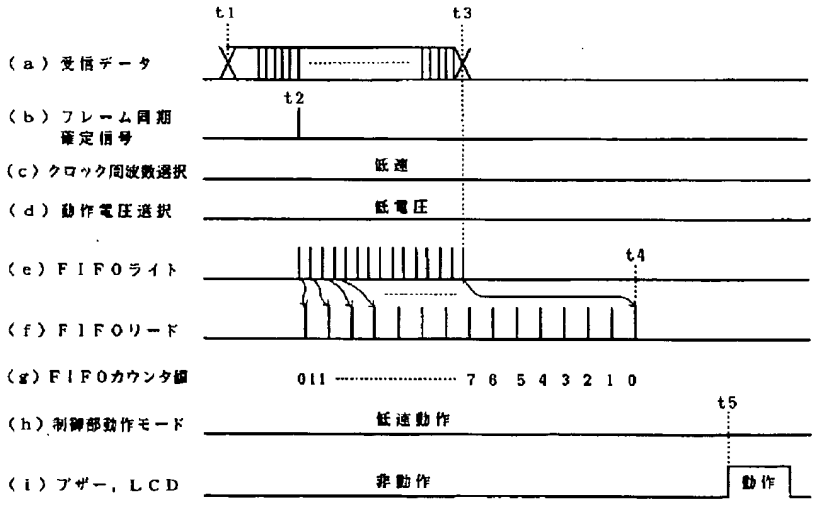
従来の信号受信処理装置ブロック図

【図4】



本発明の装置の高速モードにおける動作タイムチャート

【図5】



本発明の装置の低速モードにおける動作タイムチャート

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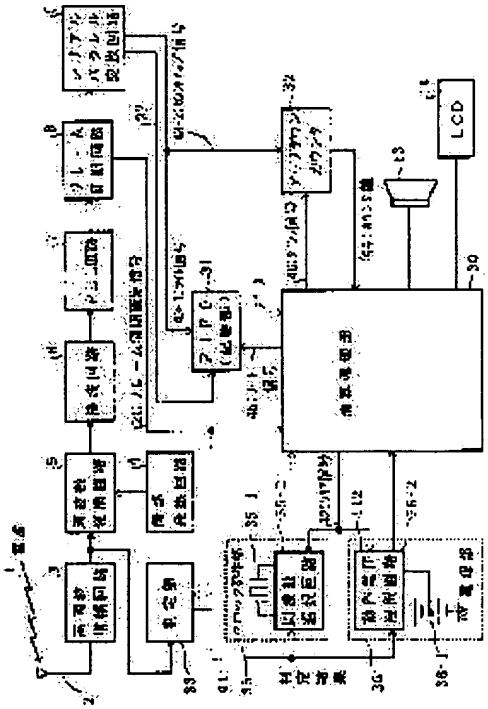
(54) SIGNAL RECEPTION PROCESSOR

(57) Abstract:
PURPOSE: To efficiently execute input signal processing while sufficiently consid ering the influence of high frequency noise generated from an operation processing part.
CONSTITUTION: When the strength of a received radio wave is strong, a clock generation part 35 increases a clock frequency, and a power supply part 36 increases an output voltage. Since the influence of high frequency noise is hardly received when the signal strength is high, operation processing is executed at high processing speed. On the other hand, when the strength of the received radio wave is weak, the level of high frequency noise is suppressed sufficiently low by reducing the clock frequency and decreasing the output voltage of the power source as well. Since the processing speed of an operation processing part 30 is lowered at such a time, the deceleration of processing speed is compensated by temporarily storing an input signal in a storage part.



LEGAL STATUS

[Date of request for examination]

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[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

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[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] It is signal reception equipment which is equipped with the following and characterized by the aforementioned power supply section choosing low output voltage when output voltage high when judged with the intensity of the aforementioned received electric wave being strong by the aforementioned judgment section is chosen and it is judged with the intensity of the aforementioned received electric wave being weak. The judgment section which detects the intensity of a received electric wave and judges the level. The data-processing section which processes the data obtained from the aforementioned received electric wave. The power supply section which chooses either among two or more sorts of output voltage to this data-processing section, and supplies the power for a drive. The storage section which accumulates it temporarily before the aforementioned data-processing section processes the signal acquired from the aforementioned received electric wave.
[Claim 2] It is signal reception equipment which is equipped with the following and characterized by the aforementioned clock generation section choosing a low clock frequency when a clock frequency high when judged with the intensity of the aforementioned received electric wave being strong by the aforementioned judgment section is chosen and it is judged with the intensity of the aforementioned received electric wave being weak. The judgment section which detects the intensity of a received electric wave and judges the level. The data-processing section which processes the data obtained from the aforementioned received electric wave. The clock generation section which chooses any they are among the clocks for operation of two or more sorts of frequency, and is supplied to this data-processing section. The storage section which accumulates it temporarily before the aforementioned data-processing section processes the signal acquired from the aforementioned received electric wave.
[Claim 3] When it has the following and the aforementioned power supply section is judged as the intensity of the aforementioned received electric wave being strong by the aforementioned judgment section When high output voltage is chosen and it is judged with the intensity of the aforementioned received electric wave being weak It is signal reception equipment characterized by choosing a low clock frequency when a clock frequency high when judged with the aforementioned clock generation section having the strong intensity of the aforementioned received electric wave is chosen and it is judged with the intensity of the aforementioned received electric wave being weak, while choosing low output voltage. The judgment section which detects the intensity of a received electric wave and judges the level. The data-processing section which processes the data obtained from the aforementioned received electric wave. The power supply section which chooses either among two or more sorts of output voltage to this data-processing section, and supplies the power for a drive. The clock generation section which chooses any they are among the clocks for operation of two or more sorts of frequency, and is supplied to the aforementioned data-processing section, and the storage section which accumulates it temporarily before the aforementioned data-processing section processes the signal acquired from the aforementioned received electric wave.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] this invention relates to the signal reception equipment for performing a call, an alarm, etc. using radio.
[0002]
[Description of the Prior Art] Although the method for transfer of the call to what is present in the distant place conventionally, or information is based on the cable using the communication line, it has some which are depended on the radio using others and the electric wave. An easy receiver is carried and what performs a call, transfer of an easy message, etc. by the electric wave is adopted widely. Moreover, equipment which performs communication of information by signal processing of a digital method is also used.
[0003] The block diagram of such conventional signal reception equipment is shown in drawing 2 . The equipment of drawing receives the electric wave 1 which carried information, such as a call and an alarm, with an antenna 2, and performs fixed processing. The RF amplifying circuit 3, the local oscillation circuit 4, a frequency changing circuit 5, a detector circuit 6, the PLL circuit 7, the frame synchronization circuit 8, and serial parallel conversion circuit 9 grade are prepared in this equipment, and it has become it with the composition which takes out fixed data from a received electric wave. Moreover, in order to process this data, the data-processing section 10 is formed, and this data-processing section 10 is driven by the power supply section 11 and the clock generation section 12. The processing result of the data-processing section 10 has composition outputted to a buzzer 13 or LCD14.
[0004] The electric wave received by this equipment puts the digital data of a fixed frame form on a medium wave, and is sent to it. The RF amplifying circuit 3 amplifies the feeble electric wave received with the antenna 2, and outputs it to a frequency changing circuit 5. The local oscillation circuit 4 outputs a signal with a local oscillation frequency of 455kHz as opposed to a frequency changing circuit 5, and a frequency changing circuit 5 changes an input signal into an intermediate frequency by this. This is operation of the medium wave receiver of a superheterodyne method known well. The output of a frequency changing circuit 5 is inputted into a detector circuit 6, and it restores to it.
[0005] In this way, although a serial fixed digital pulse signal is obtained from a detector circuit 6, this signal is inputted into the PLL circuit 7 in order to operate orthopedically the wave which produced distortion during propagation. A PLL circuit operates an input signal orthopedically to the digital signal of fixed level with a fixed period by the so-called phase locked loop. The output of this PLL circuit 7 inputs into the frame synchronization circuit 8. By this frame synchronization circuit 8, a synchronization pulse is extracted out of the frame of an input signal, and the timing of signal processing in a frame is obtained. The serial parallel conversion circuit 9 accepts the output of this frame synchronization circuit 8, changes it into a parallel data by fixed bit width of face, and is sent into the data-processing section 10.
[0006] Data extraction processing explanatory drawing from a received electric wave is shown in drawing 3 . Operation of a portion which changes an input signal into a parallel data from the above-mentioned PLL circuit 7 by the serial parallel conversion circuit 9 through the frame synchronization circuit 8 was shown in this drawing. That is, the output signal 17 of the PLL circuit 7 serves as frame form of fixed length, and the synchronizing signal 17-1 is contained in the head portion. The frame synchronization circuit 8 extracts a synchronization pulse 21-1 from this synchronizing signal 17-1, and decides the read timing of an input signal 17. This synchronous decision signal 21 is outputted towards the data-processing section 10. the serial signal which inputs the serial parallel conversion circuit 9 in this way -- for example, 4 bits -- or it starts 8 bits at a time, changes into a parallel data 22, and sends into the data-processing section 10
[0007] The data-processing section 10 decodes and analyzes the data obtained in this way, for example, the contents are displayed on LCD (liquid crystal display)14, or it sounds a buzzer 13 if needed. In addition, the power supply section 11 is equipped with the cell 11-1, and is a circuit which supplies the power for a drive to the data-processing section 10 by

turning on a switch 11-2. Moreover, the clock generation section 12 is equipped with the clock generator 12-1, and is a circuit which supplies the clock for operation operation of the data-processing section 10.
[0008]
[Problem(s) to be Solved by the Invention] By the way, with the above conventional signal reception equipments, there was a problem of blocking the electric wave 1 which it is received by the antenna 2 and the RF noise 16 generated from the data-processing section 10 originally tends to receive. Then, by making low conventionally the clock frequency which the clock generation section 12 generates to about dozens of kHz, a harmonic content is decreased and suppression of disturbance is aimed at. Moreover, the output voltage of a power supply section 11 is set as less than [3V], also reduces the signal level of a clock, and it is made to decrease the energy of a RF noise.
[0009] When it is going to make [many] amount of information at fast transmission speed when aiming at such solution for example, the processing in the data-processing section 10 stops however, meeting the deadline. That is, informational processing in which it inputted if frequency of the clock in the clock generation section 12 was made high and signal-processing speed was not raised does not meet the deadline. Therefore, when the intensity of a received electric wave was sufficiently strong, influence of a RF noise could not be disregarded but there was [except] a problem that amount of information could not be increased.
[0010] this invention was made paying attention to the above point, and aims at offering the signal reception equipment which performs input signal processing efficiently fully in consideration of the influence of the RF noise which the data-processing section generates.
[0011]
[Means for Solving the Problem] The judgment section which the 1st invention of this invention detects the intensity of a received electric wave, and judges the level, The data-processing section which processes the data obtained from the aforementioned received electric wave, and the power supply section which chooses either among two or more sorts of output voltage to this data-processing section, and supplies the power for a drive, It has the storage section which accumulates it temporarily before the aforementioned data-processing section processes the signal acquired from the aforementioned received electric wave. the aforementioned power supply section When output voltage high when judged with the intensity of the aforementioned received electric wave being strong by the aforementioned judgment section is chosen and it is judged with the intensity of the aforementioned received electric wave being weak, it is related with the signal reception equipment characterized by choosing low output voltage.
[0012] The judgment section which the 2nd invention detects the intensity of a received electric wave, and judges the level, The data-processing section which processes the data obtained from the aforementioned received electric wave, and the clock generation section which chooses any they are among the clocks for operation of two or more sorts of frequency, and is supplied to this data-processing section, It has the storage section which accumulates it temporarily before the aforementioned data-processing section processes the signal acquired from the aforementioned received electric wave. the aforementioned clock generation section When a clock frequency high when judged with the intensity of the aforementioned received electric wave being strong by the aforementioned judgment section is chosen and it is judged with the intensity of the aforementioned received electric wave being weak, it is related with the signal reception equipment characterized by choosing a low clock frequency.
[0013] The judgment section which the 3rd invention detects the intensity of a received electric wave, and judges the level, The data-processing section which processes the data obtained from the aforementioned received electric wave, and the power supply section which chooses either among two or more sorts of output voltage to this data-processing section, and supplies the power for a drive, The clock generation section which chooses any they are among the clocks for operation of two or more sorts of frequency, and is supplied to the aforementioned data-processing section, It has the storage section which accumulates it temporarily before the aforementioned data-processing section processes the signal acquired from the aforementioned received electric wave. the aforementioned power supply section When judged with the intensity of the aforementioned received electric wave being strong by the aforementioned judgment section When high output voltage is chosen and it is judged with the intensity of the aforementioned received electric wave being weak While choosing low output voltage, when a clock frequency high when judged with the aforementioned clock generation section having the strong intensity of the aforementioned received electric wave is chosen and it is judged with the intensity of the aforementioned received electric wave being weak, it is related with the signal reception equipment characterized by choosing a low clock frequency.
[0014]
[Function] With this equipment, when the intensity of a received electric wave is strong, the clock generation section makes a clock frequency high, and a power supply section raises output voltage. Since it is hard to be influenced of a RF

noise when signal strength is strong, data processing is performed with high processing speed by this. Conversely, when the intensity of a received electric wave is weak, a clock frequency is reduced, and output voltage of a power supply is also made low and stops the level of a RF noise. When an input signal is fast transmission mode, this is once accumulated in the storage section and the processing speed fall of the data-processing section is compensated.

[0015]

[Example] Hereafter, this invention is explained in detail using the example of drawing. Drawing 1 is the block diagram showing the signal reception equipment example of this invention. The equipment of drawing is equipped with an antenna 2, the RF amplifying circuit 3, the local oscillation circuit 4, a frequency changing circuit 5, the detector circuit 6, the PLL circuit 7, the frame synchronization circuit 8, and the serial parallel conversion circuit 9 like the conventional equipment explained using drawing 2 . Moreover, in order to process the data obtained by these circuits, the data-processing section 30 is formed, and the processing result has composition outputted to a buzzer 13 or LCD14. There are not equipment of the former [composition / so far] and a changing place. Here, since the data 22 which the serial parallel conversion circuit 9 outputs are stored in the equipment of this invention temporarily, FIFO (FIFO memory)31 is formed. In this invention, this FIFO31 is called storage section. Moreover, in order to manage the data stored in this FIFO31, the updown counter 32 is formed.

[0016] On the other hand, it is outputted towards a frequency changing circuit 5, and also the output of the RF amplifying circuit 3 is constituted so that it may input into the judgment section 33 for detecting the intensity of a received electric wave and judging the level. Moreover, the judgment result 41 which this judgment section 33 outputs is constituted so that it may input into the clock generation section 35 and a power supply section 36. The clock generator 35-1 and the frequency-selective circuit 35-2 are established in the clock generation section 35. The frequency-selective circuit 35-2 switches the frequency of the clock supplied to the data-processing section 30 to two stages, for example in this example, and has composition which can choose and output either of the clocks of high frequency and low frequency. The circuit for selection of this frequency is constituted by the switch which chooses the output of the frequency divider prepared in the frequency changing circuit 35-2. Thereby, this clock generation section 35 has composition which can choose and output a clock with a low frequency of the dozens of same kHz [as usual], or the double precision or several times as many clock as this.

[0017] On the other hand, the cell 36-1 and the operating voltage selection circuitry 36-2 are formed in the power supply section 36. This operating voltage selection circuitry 36-2 switches the output of a cell 36-1 with a switch, for example, is considered as the composition which can choose and output either among two kinds of output voltage, 3V and 4.5V. In addition, although the frame synchronization decision signal 21 is outputted conventionally like equipment from the frame synchronization circuit 8, this signal is inputted also into the judgment section 33, and the judgment section 33 is considered as the composition which outputs the judgment result 41 to the timing which this frame synchronization decision signal 21 inputs. The judgment section 33 specifically consists of a comparator circuit [signal / which the RF amplifying circuit 3 outputs / a fixed reference value], a gate circuit which outputs the comparison result to the clock generation section 35 or a power supply section 36 by control of the frame synchronization decision signal 21.

[0018] FIFO31 is accepted to the timing into which the light signal 43-1 inputs the data outputted from the serial parallel conversion circuit 9, and consists of memory accumulated in order. In this way, the accumulated data are read towards the data-processing section 30 by the lead signal 45 outputted from the data-processing section 30. The storage capacity of this FIFO31 is set as the suitable amount which can accumulate the superfluous part, when the amount of information of an input signal exceeds the amount of information processing per unit time of the data-processing section 30. An updown counter 32 is a counter constituted by the input of the down signal 46 so that the counter value might be made downed every [1], whenever it accepts the count-up signal 43-2 outputted from the serial parallel conversion circuit 9, it raises the counter value every [1] whenever one data is stored in FIFO31, and the data-processing section 30 reads one data from FIFO31. The counter value 44 which an updown counter 32 outputs is outputted towards the data-processing section 30, and the data-processing section 30 has the composition that the amount of the remaining data stored in FIFO31 with this counter value 44 can be recognized.

[0019] In addition, in order for each to return operation of the frequency-selective circuit 35-2 or the operating voltage selection circuitry 36-2 to initial value, it is constituted by the clock generation section 35 and the power supply section 36 so that the clear signal 42 may input. The data-processing section 30 turns and outputs this clear signal 42 to the clock generation section 35 or a power supply section 36 to predetermined timing, and it is constituted so that an initial state may be set up.

[0020] Hereafter, operation of the equipment of this invention is explained. First, connection of the switch which a power supply section 36 does not illustrate supplies power to a circuit by the output voltage of the initial state set up beforehand.

This voltage shall be set, for example as the level of the lower one. Moreover, the clock generation section 35 generates a clock in the clock frequency of the lower one as an initial state, and supplies it to the data-processing section 30. Here, if an antenna 2 receives an electric wave 1, the RF amplifying circuit 3 will amplify the electric wave. The output is inputted into a frequency changing circuit 5 and the judgment section 33. A frequency changing circuit 5 generates an intermediate frequency by the output of the local oscillation circuit 4, and a detector circuit 6 restores to the signal. The PLL circuit 7 operates the wave of an input signal orthopedically, and synchronous processing is performed in the frame synchronization circuit 8. These are the same operation as the conventional equipment already explained using drawing 2.

[0021] Here, as it explained previously that the frame synchronization decision signal 21 was outputted from the frame synchronization circuit 8, the judgment section 33 outputs the judgment result 41 which judged the level of the signal which the RF amplifying circuit 3 outputs to the timing to the clock generation section 35 and a power supply section 36. The frequency-selective circuit 35-2 of the clock generation section 35 and the operating voltage selection circuitry 36-2 of a power supply section 36 choose the frequency and output voltage of a clock according to this judgment result 41, respectively. Low, the clock frequency for the signal processing is maintained by the voltage which follows, for example, drives the data-processing section 30 when the level of a received electric wave is low as it is low. On the other hand, when the intensity of a received electric wave is strong, the output voltage of a power supply section 36 rises, the clock frequency which the clock generation section 35 generates is set up highly, and the data-processing section 30 operates by fast mode.

[0022] The timing diagram of operation in the fast mode of the equipment of this invention is shown in drawing 4 . As were shown in (a) of drawing, and received data were received at time t1 and it was shown in (b), the frame synchronization decision signal should be outputted to time t2 from the frame synchronization circuit 8. In this case, the clock generation section 35 and a power supply section 36 choose a clock frequency and operating voltage, as shown in (c) of drawing 4 , and (d). In this example, a clock frequency is chosen at high speed and operating voltage is chosen as the high voltage.

[0023] In this state, the serial parallel conversion circuit 9 writes in the data which carried out parallel conversion towards FIFO31 (this drawing (e)). The frame synchronization decision signal 21 has inputted into the data-processing section 30 from the frame synchronization circuit 8 (this drawing (f)), and the data-processing section 30 starts read-out of data from FIFO31 to the timing in it. Although the frame of received data is received during time t1 - time t4 as shown in drawing 4 (a), the data-processing section 30 processes data in fast mode from time t2, and at time t5, based on the processing result, a buzzer 13 is driven or it displays a processing result on LCD14 (this drawing (h)). After processing is completed, the data-processing section 30 outputs the clear signal 42 to time t6, and directs the clock frequency of the clock generation section 35 and a power supply section 36, and the change of operating voltage (this drawing (g)).

[0024] Thus, when judging the intensity of a received electric wave, setting initial value as a low clock frequency by low output voltage makes low enough the RF noise which the data-processing section 30 generates, and it is for not performing the mistaken judgment. For example, a microcomputer (8 bits or 4 bits) is usually used for the above-mentioned data-processing section 30. Although the range of the clock of operation was 1MHz - about 5MHz, in order to stop a RF noise sufficiently low, it had selected the clock frequency to dozens of kHz in this kind of signal reception equipment. In addition, supply voltage was set as about 1.5V-3V in this case.

[0025] In such the state, data transfer speed is restricted to about 512bps at the maximum. However, if a clock frequency is not selected to about several MHz when a data transfer rate is about 4800bps, for example, processing does not meet the deadline. Moreover, processing for this kind of data coding data so that highness and lows may be scattered equally in order that PLL may not operate, if the state of scramble processing, i.e., the highness of a data bit, or a low continues is performed. Therefore, since error correction processing etc. is performed after decode of such data and actual data processing is performed after that, there are many throughputs, and the response itself will become remarkably late when a clock of operation is late. Therefore, such a problem is solvable by enabling operation by the above fast modes.

[0026] On the other hand, when the intensity of a received electric wave is weak, the equipment of this invention operates as follows. The timing diagram of operation in the slow mode of the equipment of this invention is shown in drawing 5 . As shown in drawing 5 (a), reception of data shall be performed during time t1 - time t3, and a frame synchronization decision signal shall be outputted to time t2 (this drawing (b)). In this case, if the intensity of a received electric wave is weak, according to the judgment result 41 of the judgment section 33, the clock generation section 35 chooses the clock of low frequency, and a power supply section 36 will choose low voltage, and it will supply it to the data-processing section 30 (this drawing (c), (d)). The RF noise which the data-processing section 30 generates is set as sufficiently low level by this, and has the disturbance to a received electric wave suppressed.

[0027] On the other hand, as for the data-processing section 30, the processing speed falls by the fall of a clock frequency. Therefore, if the data outputted from the serial parallel conversion circuit 9 are received as it is, the case where processing does not meet the deadline is generated. Then, the data inputted into FIFO31 from the serial parallel conversion circuit 9 are once accumulated, and the data-processing section 30 calls and processes the data from FIFO31 according to the set-up processing speed. It comes to indicate the relation to be drawing 5 (e) to (f). That is, although the received data will be stored in FIFO31 by time t3, the data-processing section 30 reads data to before time t4 after that, and performs data processing. An updown counter 32 counts the amount of the data stored in FIFO31 in the meantime (this drawing (g)), and the data-processing section 30 manages the amount of the power data to read. Consequently, the processing result of the data-processing section 30 is outputted to a buzzer 13 or LCD14 at time t5 (this drawing (i)).
[0028] Although operation processing speed falls and the speed of response of equipment becomes slow by switching a clock frequency low so that drawing 4 and drawing 5 may be compared and understood, since received data are temporarily memorized by FIFO31, the data-processing section 30 operates certainly and outputs a required processing result. Therefore, in the place where electric field are weak, the obstacle of producing the receiving error of a signal by the noise, or processing stopping meeting the deadline and malfunctioning since the transfer rate of a signal is early can also be prevented.
[0029] this invention is not limited to the above example. In the above-mentioned example, it is with the case where the level of a received electric wave is high, and the case of being low, and it switched so that the frequency of a clock and the output voltage of a power supply section 36 which the clock generation section 35 outputs might be simultaneously made high or it might be made low. However, supply voltage which a power supply section 36 outputs, for example is fixed, and even if it changes only the frequency of the clock which the clock generation section 35 outputs, it does not interfere. The change number of stages may be made to be switched freely not two stages but more than a three-stage. Therefore, the output voltage of the clock frequency which the clock generation section 35 outputs, or a power supply section 36 may be switched to how many step story it is separately independently, respectively, and you may constitute in the range which is not large so that the data-processing section 30 may be driven in the optimal state. Moreover, with the property of the signal sent by the electric wave, the composition of a receiving circuit can be changed freely, and cannot interfere, and the control methods, such as the storage section, and the clock generation section, a power supply section, can be freely changed by the circuitry. Moreover, the processing result of the data-processing section can apply this invention also about what controls operation of a certain equipment directly based on its result besides in the case of displaying on a buzzer, LCD, etc.
[0030]
[Effect of the Invention] The signal reception equipment of this invention explained above detects the intensity of a received electric wave, and judges the level by the judgment section. when the intensity of a received electric wave is strong The output voltage of a power supply section is chosen highly, and the clock frequency of the clock generation section is chosen highly. when the intensity of a received electric wave is weak Since the clock frequency which the output voltage of a power supply section is low selected, and the clock generation section outputs is chosen low, the RF noise which the data-processing section always generates can be held down to the level which does not influence reception operation, and positive signal processing can be performed. Therefore, when the intensity of a received electric wave is high, signal processing can be performed at high speed and a lot of information can be processed promptly. Moreover, when the intensity of a received electric wave is weak, a RF noise is stopped low automatically, and it becomes certain operating it in order to compensate the fall of processing speed by accumulating data in the storage section temporarily.
[0031] Furthermore, in the usual state, in order to make a clock frequency and operating voltage low, when power consumption is mitigated and it drives using a cell etc., the uptime can be lengthened. Moreover, although it sees from the operation top of the data-processing section, or the RF noise mitigation effect and a limitation is in the adjustable range when only a clock frequency is adjusted, there is an effect which can choose a mode of operation in the large range by changing a clock frequency and supply voltage simultaneously. Moreover, also by easy control to which only operating voltage is changed, a RF noise is adjusted in the fixed range and reception operation in the optimal state can be secured.

[Translation done.]

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TECHNICAL FIELD

[Industrial Application] this invention relates to the signal reception equipment for performing a call, an alarm, etc. using radio.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Although the method for transfer of the call to what is present in the distant place conventionally, or information is based on the cable using the communication line, it has some which are depended on the radio using others and the electric wave. An easy receiver is carried and what performs a call, transfer of an easy message, etc. by the electric wave is adopted widely. Moreover, equipment which performs communication of information by signal processing of a digital method is also used.

[0003] The block diagram of such conventional signal reception equipment is shown in drawing 2 . The equipment of drawing receives the electric wave 1 which carried information, such as a call and an alarm, with an antenna 2, and performs fixed processing. The RF amplifying circuit 3, the local oscillation circuit 4, a frequency changing circuit 5, a detector circuit 6, the PLL circuit 7, the frame synchronization circuit 8, and serial parallel conversion circuit 9 grade are prepared in this equipment, and it has become it with the composition which takes out fixed data from a received electric wave. Moreover, in order to process this data, the data-processing section 10 is formed, and this data-processing section 10 is driven by the power supply section 11 and the clock generation section 12. The processing result of the data-processing section 10 has composition outputted to a buzzer 13 or LCD14.

[0004] The electric wave received by this equipment puts the digital data of a fixed frame form on a medium wave, and is sent to it. The RF amplifying circuit 3 amplifies the feeble electric wave received with the antenna 2, and outputs it to a frequency changing circuit 5. The local oscillation circuit 4 outputs a signal with a local oscillation frequency of 455kHz as opposed to a frequency changing circuit 5, and a frequency changing circuit 5 changes an input signal into an intermediate frequency by this. This is operation of the medium wave receiver of a superheterodyne method known well. The output of a frequency changing circuit 5 is inputted into a detector circuit 6, and it restores to it.

[0005] In this way, although a serial fixed digital pulse signal is obtained from a detector circuit 6, this signal is inputted into the PLL circuit 7 in order to operate orthopedically the wave which produced distortion during propagation. A PLL circuit operates an input signal orthopedically to the digital signal of fixed level with a fixed period by the so-called phase locked loop. The output of this PLL circuit 7 inputs into the frame synchronization circuit 8. By this frame synchronization circuit 8, a synchronization pulse is extracted out of the frame of an input signal, and the timing of signal processing in a frame is obtained. The serial parallel conversion circuit 9 accepts the output of this frame synchronization circuit 8, changes it into a parallel data by fixed bit width of face, and is sent into the data-processing section 10.

[0006] Data extraction processing explanatory drawing from a received electric wave is shown in drawing 3 . Operation of a portion which changes an input signal into a parallel data from the above-mentioned PLL circuit 7 by the serial parallel conversion circuit 9 through the frame synchronization circuit 8 was shown in this drawing. That is, the output signal 17 of the PLL circuit 7 serves as frame form of fixed length, and the synchronizing signal 17-1 is contained in the head portion. The frame synchronization circuit 8 extracts a synchronization pulse 21-1 from this synchronizing signal 17-1, and decides the read timing of an input signal 17. This synchronous decision signal 21 is outputted towards the data-processing section 10. the serial signal which inputs the serial parallel conversion circuit 9 in this way -- for example, 4 bits -- or it starts 8 bits at a time, changes into a parallel data 22, and sends into the data-processing section 10

[0007] The data-processing section 10 decodes and analyzes the data obtained in this way, for example, the contents are displayed on LCD (liquid crystal display)14, or it sounds a buzzer 13 if needed. In addition, the power supply section 11 is equipped with the cell 11-1, and is a circuit which supplies the power for a drive to the data-processing section 10 by turning on a switch 11-2. Moreover, the clock generation section 12 is equipped with the clock generator 12-1, and is a circuit which supplies the clock for operation operation of the data-processing section 10.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] The signal reception equipment of this invention explained above detects the intensity of a received electric wave, judges the level by the judgment section, and when the intensity of a received electric wave is strong, it is. It can hold down to the level which does not influence reception operation in the RF noise which the data-processing section always generates since the clock frequency which the output voltage of a power supply section is highly chosen, and the clock frequency of the clock generation section is highly chosen, the output voltage of a power supply section is low selected when the intensity of a received electric wave is weak, and the clock generation section outputs is chosen low, and positive signal processing can be performed. Therefore, when the intensity of a received electric wave is high, signal processing can be performed at high speed and a lot of information can be processed promptly. Moreover, when the intensity of a received electric wave is weak, a RF noise is stopped low automatically, and it becomes certain operating it in order to compensate the fall of processing speed by accumulating data in the storage section temporarily.

[0031] Furthermore, in the usual state, in order to make a clock frequency and operating voltage low, when power consumption is mitigated and it drives using a cell etc., the uptime can be lengthened. Moreover, although it sees from the operation top of the data-processing section, or the RF noise mitigation effect and a limitation is in the adjustable range when only a clock frequency is adjusted, there is an effect which can choose a mode of operation in the large range by changing a clock frequency and supply voltage simultaneously. Moreover, also by easy control to which only operating voltage is changed, a RF noise is adjusted in the fixed range and reception operation in the optimal state can be secured.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] By the way, with the above conventional signal reception equipments, there was a problem of blocking the electric wave 1 which it is received by the antenna 2 and the RF noise 16 generated from the data-processing section 10 originally tends to receive. Then, by making low conventionally the clock frequency which the clock generation section 12 generates to about dozens of kHz, a harmonic content is decreased and suppression of disturbance is aimed at. Moreover, the output voltage of a power supply section 11 is set as less than [3V], also reduces the signal level of a clock, and it is made to decrease the energy of a RF noise.

[0009] When it is going to make [many] amount of information at fast transmission speed when aiming at such solution for example, the processing in the data-processing section 10 stops however, meeting the deadline. That is, informational processing in which it inputted if frequency of the clock in the clock generation section 12 was made high and signal-processing speed was not raised does not meet the deadline. Therefore, when the intensity of a received electric wave was sufficiently strong, influence of a RF noise could not be disregarded but there was [except] a problem that amount of information could not be increased.

[0010] this invention was made paying attention to the above point, and aims at offering the signal reception equipment which performs input signal processing efficiently fully in consideration of the influence of the RF noise which the data-processing section generates.

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MEANS

[Means for Solving the Problem] The judgment section which the 1st invention of this invention detects the intensity of a received electric wave, and judges the level, The data-processing section which processes the data obtained from the aforementioned received electric wave, and the power supply section which chooses either among two or more sorts of output voltage to this data-processing section, and supplies the power for a drive, It has the storage section which accumulates it temporarily before the aforementioned data-processing section processes the signal acquired from the aforementioned received electric wave. the aforementioned power supply section When output voltage high when judged with the intensity of the aforementioned received electric wave being strong by the aforementioned judgment section is chosen and it is judged with the intensity of the aforementioned received electric wave being weak, it is related with the signal reception equipment characterized by choosing low output voltage.

[0012] The judgment section which the 2nd invention detects the intensity of a received electric wave, and judges the level, The data-processing section which processes the data obtained from the aforementioned received electric wave, and the clock generation section which chooses any they are among the clocks for operation of two or more sorts of frequency, and is supplied to this data-processing section, It has the storage section which accumulates it temporarily before the aforementioned data-processing section processes the signal acquired from the aforementioned received electric wave. the aforementioned clock generation section When a clock frequency high when judged with the intensity of the aforementioned received electric wave being strong by the aforementioned judgment section is chosen and it is judged with the intensity of the aforementioned received electric wave being weak, it is related with the signal reception equipment characterized by choosing a low clock frequency.

[0013] The judgment section which the 3rd invention detects the intensity of a received electric wave, and judges the level, The data-processing section which processes the data obtained from the aforementioned received electric wave, and the power supply section which chooses either among two or more sorts of output voltage to this data-processing section, and supplies the power for a drive, The clock generation section which chooses any they are among the clocks for operation of two or more sorts of frequency, and is supplied to the aforementioned data-processing section, It has the storage section which accumulates it temporarily before the aforementioned data-processing section processes the signal acquired from the aforementioned received electric wave. the aforementioned power supply section When judged with the intensity of the aforementioned received electric wave being strong by the aforementioned judgment section When high output voltage is chosen and it is judged with the intensity of the aforementioned received electric wave being weak While choosing low output voltage, when a clock frequency high when judged with the aforementioned clock generation section having the strong intensity of the aforementioned received electric wave is chosen and it is judged with the intensity of the aforementioned received electric wave being weak, it is related with the signal reception equipment characterized by choosing a low clock frequency.

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OPERATION

[Function] With this equipment, when the intensity of a received electric wave is strong, the clock generation section makes a clock frequency high, and a power supply section raises output voltage. Since it is hard to be influenced of a RF noise when signal strength is strong, data processing is performed with high processing speed by this. Conversely, when the intensity of a received electric wave is weak, a clock frequency is reduced, and output voltage of a power supply is also made low and stops the level of a RF noise. When an input signal is fast transmission mode, this is once accumulated in the storage section and the processing speed fall of the data-processing section is compensated.

[Translation done.]

* NOTICES *

EXAMPLE

[Example] Hereafter, this invention is explained in detail using the example of drawing. Drawing 1 is the block diagram showing the signal reception equipment example of this invention. The equipment of drawing is equipped with an antenna 2, the RF amplifying circuit 3, the local oscillation circuit 4, a frequency changing circuit 5, the detector circuit 6, the PLL circuit 7, the frame synchronization circuit 8, and the serial parallel conversion circuit 9 like the conventional equipment explained using drawing 2 . Moreover, in order to process the data obtained by these circuits, the data-processing section 30 is formed, and the processing result has composition outputted to a buzzer 13 or LCD14. There are not equipment of the former [composition / so far] and a changing place. Here, since the data 22 which the serial parallel conversion circuit 9 outputs are stored in the equipment of this invention temporarily, FIFO (FIFO memory)31 is formed. In this invention, this FIFO31 is called storage section. Moreover, in order to manage the data stored in this FIFO31, the updown counter 32 is formed.

[0016] On the other hand, it is outputted towards a frequency changing circuit 5, and also the output of the RF amplifying circuit 3 is constituted so that it may input into the judgment section 33 for detecting the intensity of a received electric wave and judging the level. Moreover, the judgment result 41 which this judgment section 33 outputs is constituted so that it may input into the clock generation section 35 and a power supply section 36. The clock generator 35-1 and the frequency-selective circuit 35-2 are established in the clock generation section 35. The frequency-selective circuit 35-2 switches the frequency of the clock supplied to the data-processing section 30 to two stages, for example in this example, and has composition which can choose and output either of the clocks of high frequency and low frequency. The circuit for selection of this frequency is constituted by the switch which chooses the output of the frequency divider prepared in the frequency changing circuit 35-2. Thereby, this clock generation section 35 has composition which can choose and output a clock with a same low frequency [the / as usual] of dozens of kHz, or the double precision or several times as many clock as this.

[0017] On the other hand, the cell 36-1 and the operating voltage selection circuitry 36-2 are formed in the power supply section 36. This operating voltage selection circuitry 36-2 switches the output of a cell 36-1 with a switch, for example, is considered as the composition which can choose and output either among two kinds of output voltage, 3V and 4.5V. In addition, although the frame synchronization decision signal 21 is outputted conventionally like equipment from the frame synchronization circuit 8, this signal is inputted also into the judgment section 33, and the judgment section 33 is considered as the composition which outputs the judgment result 41 to the timing which this frame synchronization decision signal 21 inputs. The judgment section 33 specifically consists of a comparator circuit [signal / which the RF amplifying circuit 3 outputs / a fixed reference value], a gate circuit which outputs the comparison result to the clock generation section 35 or a power supply section 36 by control of the frame synchronization decision signal 21.

[0018] FIFO31 is accepted to the timing into which the light signal 43-1 inputs the data outputted from the serial parallel conversion circuit 9, and consists of memory accumulated in order. In this way, the accumulated data are read towards the data-processing section 30 by the lead signal 45 outputted from the data-processing section 30. The storage capacity of this FIFO31 is set as the suitable amount which can accumulate the superfluous part, when the amount of information of an input signal exceeds the amount of information processing per unit time of the data-processing section 30. An updown counter 32 is a counter constituted by the input of the down signal 46 so that the counter value might be made downed every [1], whenever it accepts the count-up signal 43-2 outputted from the serial parallel conversion circuit 9, it raises the counter value every [1] whenever one data is stored in FIFO31, and the data-processing section 30 reads one data from FIFO31. The counter value 44 which an updown counter 32 outputs is outputted towards the data-processing section 30, and the data-processing section 30 has the composition that the amount of the remaining data stored in FIFO31 with this counter value 44 can be recognized.

[0019] In addition, in order for each to return operation of the frequency-selective circuit 35-2 or the operating voltage

selection circuitry 36-2 to initial value, it is constituted by the clock generation section 35 and the power supply section 36 so that the clear signal 42 may input. The data-processing section 30 turns and outputs this clear signal 42 to the clock generation section 35 or a power supply section 36 to predetermined timing, and it is constituted so that an initial state may be set up.

[0020] Hereafter, operation of the equipment of this invention is explained. First, connection of the switch which a power supply section 36 does not illustrate supplies power to a circuit by the output voltage of the initial state set up beforehand. This voltage shall be set as the level of for example, the method of a low. Moreover, the clock generation section 35 generates a clock in the clock frequency of the method of a low as an initial state, and supplies it to the data-processing section 30. Here, if an antenna 2 receives an electric wave 1, the RF amplifying circuit 3 will amplify the electric wave. The output is inputted into a frequency changing circuit 5 and the judgment section 33. A frequency changing circuit 5 generates an intermediate frequency by the output of the local oscillation circuit 4, and a detector circuit 6 restores to the signal. The PLL circuit 7 operates the wave of an input signal orthopedically, and synchronous processing is performed in the frame synchronization circuit 8. These are the same operation as the conventional equipment already explained using drawing 2 .

[0021] Here, as it explained previously that the frame synchronization decision signal 21 was outputted from the frame synchronization circuit 8, the judgment section 33 outputs the judgment result 41 which judged the level of the signal which the RF amplifying circuit 3 outputs to the timing to the clock generation section 35 and a power supply section 36. The frequency-selective circuit 35-2 of the clock generation section 35 and the operating voltage selection circuitry 36-2 of a power supply section 36 choose the frequency and output voltage of a clock according to this judgment result 41, respectively. Low, the clock frequency for the signal processing is maintained by the voltage which follows, for example, drives the data-processing section 30 when the level of a received electric wave is low as it is low. On the other hand, when the intensity of a received electric wave is strong, the output voltage of a power supply section 36 rises, the clock frequency which the clock generation section 35 generates is set up highly, and the data-processing section 30 operates by fast mode.

[0022] The timing diagram of operation in the fast mode of the equipment of this invention is shown in drawing 4 . As were shown in (a) of drawing, and received data were received at time t1 and it was shown in (b), the frame synchronization decision signal should be outputted to time t2 from the frame synchronization circuit 8. In this case, the clock generation section 35 and a power supply section 36 choose a clock frequency and operating voltage, as shown in (c) of drawing 4 , and (d). In this example, a clock frequency is chosen at high speed and operating voltage is chosen as the high voltage.

[0023] In this state, the serial parallel conversion circuit 9 writes in the data which carried out parallel conversion towards FIFO31 (this drawing (e)). The frame synchronization decision signal 21 has inputted into the data-processing section 30 from the frame synchronization circuit 8 (this drawing (f)), and the data-processing section 30 starts read-out of data from FIFO31 to the timing in it. Although the frame of received data is received during time t1 - time t4 as shown in drawing 4 (a), the data-processing section 30 processes data in fast mode from time t2, and at time t5, based on the processing result, a buzzer 13 is driven or it displays a processing result on LCD14 (this drawing (h)). After processing is completed, the data-processing section 30 outputs the clear signal 42 to time t6, and directs the clock frequency of the clock generation section 35 and a power supply section 36, and the change of operating voltage (this drawing (g)).

[0024] Thus, when judging the intensity of a received electric wave, setting initial value as a low clock frequency by low output voltage makes low enough the RF noise which the data-processing section 30 generates, and it is for not performing the mistaken judgment. For example, a microcomputer (8 bits or 4 bits) is usually used for the above-mentioned data-processing section 30. Although the range of the clock of operation was 1MHz - about 5MHz, in order to stop a RF noise sufficiently low, it had selected the clock frequency to dozens of kHz in this kind of signal reception equipment. In addition, supply voltage was set as about 1.5V-3V in this case.

[0025] In such the state, data transfer speed is restricted to about 512bps at the maximum. However, if a clock frequency is not selected to about several MHz when a data transfer rate is about 4800bps, for example, processing does not meet the deadline. Moreover, processing for this kind of data coding data so that highness and lows may be scattered equally in order that PLL may not operate, if the state of scramble processing, i.e., the highness of a data bit, or a low continues is performed. Therefore, since error correction processing etc. is performed after decode of such data and actual data processing is performed after that, there are many throughputs, and the response itself will become remarkably late when a clock of operation is late. Therefore, such a problem is solvable by enabling operation by the above fast modes.

[0026] On the other hand, when the intensity of a received electric wave is weak, the equipment of this invention operates as follows. The timing diagram of operation in the slow mode of the equipment of this invention is shown in drawing 5 .

As shown in drawing 5 (a), reception of data shall be performed during time t1 - time t3, and a frame synchronization decision signal shall be outputted to time t2 (this drawing (b)). In this case, if the intensity of a received electric wave is weak, according to the judgment result 41 of the judgment section 33, the clock generation section 35 chooses the clock of low frequency, and a power supply section 36 will choose low voltage, and it will supply it to the data-processing section 30 (this drawing (c), (d)). The RF noise which the data-processing section 30 generates is set as sufficiently low level by this, and has the disturbance to a received electric wave suppressed.

[0027] On the other hand, as for the data-processing section 30, the processing speed falls by the fall of a clock frequency. Therefore, if the data outputted from the serial parallel conversion circuit 9 are received as it is, the case where processing does not meet the deadline is generated. Then, the data inputted into FIFO31 from the serial parallel conversion circuit 9 are once accumulated, and the data-processing section 30 calls and processes the data from FIFO31 according to the set-up processing speed. It comes to indicate the relation to be drawing 5 (e) to (f). That is, although the received data will be stored in FIFO31 by time t3, the data-processing section 30 reads data to before time t4 after that, and performs data processing. An updown counter 32 counts the amount of the data stored in FIFO31 in the meantime (this drawing (g)), and the data-processing section 30 manages the amount of the power data to read. Consequently, the processing result of the data-processing section 30 is outputted to a buzzer 13 or LCD14 at time t5 (this drawing (i)).

[0028] Although operation processing speed falls and the speed of response of equipment becomes slow by switching a clock frequency low so that drawing 4 and drawing 5 may be compared and understood, since received data are temporarily memorized by FIFO31, the data-processing section 30 operates certainly and outputs a required processing result. Therefore, in the place where electric field are weak, the obstacle of producing the receiving error of a signal by the noise, or processing stopping meeting the deadline and malfunctioning since the transfer rate of a signal is early can also be prevented.

[0029] this invention is not limited to the above example. In the above-mentioned example, it is with the case where the level of a received electric wave is high, and the case of being low, and it switched so that the frequency of a clock and the output voltage of a power supply section 36 which the clock generation section 35 outputs might be simultaneously made high or it might be made low. However, supply voltage which a power supply section 36 outputs, for example is fixed, and even if it changes only the frequency of the clock which the clock generation section 35 outputs, it does not interfere. The change number of stages may be made to be switched freely not two stages but more than a three-stage. Therefore, the output voltage of the clock frequency which the clock generation section 35 outputs, or a power supply section 36 may be switched to how many step story it is separately independently, respectively, and you may constitute in the range which is not large so that the data-processing section 30 may be driven in the optimal state. Moreover, with the property of the signal sent by the electric wave, the composition of a receiving circuit can be changed freely, and cannot interfere, and the control methods, such as the storage section, and the clock generation section, a power supply section, can be freely changed by the circuitry. Moreover, the processing result of the data-processing section can apply this invention also about what controls operation of a certain equipment directly based on its result besides in the case of displaying on a buzzer, LCD, etc.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing the signal reception equipment example of this invention.
[Drawing 2] It is the conventional signal reception equipment block diagram.
[Drawing 3] It is data extraction processing explanatory drawing from a received electric wave.
[Drawing 4] It is a timing diagram of operation in the fast mode of the equipment of this invention.
[Drawing 5] It is a timing diagram of operation in the slow mode of the equipment of this invention.
[Description of Notations]
30 Data-Processing Section
31 FIFO (Storage Section)
33 Judgment Section
35 Clock Generation Section
36 Power Supply Section

[Translation done.]